PUB-NO: JP409148301A
DOCUMENT-IDENTIFIER: JP 09148301 A
TITLE: MANUFACTURE OF SEMICONDUCTOR DEVICE, AND ETCHANT

PUBN-DATE: June 6, 1997

INVENTOR-INFORMATION:

NAME	COUNTRY
OKAMURA, MASAO	

INT-CL (IPC): H01 L 21/306; H01 L 21/308; H01 L 21/768

ABSTRACT:

PROBLEM TO BE SOLVED: To remove spontaneous oxide from the bottom of a contact hole while preventing irregularities on the walls of the contact hole by using an aqueous etchant that has a specific concentration range of HF and a higher concentration of NH4F than specified.

SOLUTION: A thermal SiO2 film 3, a BPSG film 4-1, an atmospheric CVD SiO2 film 5, and a BPSG film 4-2 are successively deposited on a silicon substrate 2, and a contact hole 1A of 0.35 micron in diameter is opened by dry etching. Spontaneous oxide occurring on the bottom of the contact hole is etched by buffered hydrofluoric acid that contains 0-0.5wt.% HF and 37wt.% or more NH4F. In this case, the etch rate is adequately as low as 1nm/min and well- controlled etching can be performed to reduce irregularities appearing on the walls of the contact hole.

L8: Entry 2 of 2 File: DWPI Jun 6, 1997

102/103-(1-2)

DERWENT-ACC-NO: 1997-356551
DERWENT-WEEK: 199733

TITLE: Semiconductor device mfr. - involves using etching reagent consisting of ammonium fluoride, hydrogen fluoride and water, for removing natural oxide film

PRIORITY-DATA: 1995JP-0311229 (November 29, 1995)

Okamura

Search Selected | Search ALL | Clear

PATENT-FAMILY:

	PUB-NO	PUB-DATE	LANGUAGE	PAGES	MAIN-IPC
☐	JP 09148301 A	June 6, 1997		004	H01L021/306

INT-CL (IPC): H01 L 21/306; H01 L 21/308; H01 L 21/768

ABSTRACTED-PUB-NO: JP 09148301A
BASIC-ABSTRACT:

The method involves forming a multilayer structure comprising two kinds of silicon oxide insulating films on a semiconductor substrate. A contact hole is formed in the multilayer structure thus exposing semiconductor substrate.

The natural oxide film on the exposed surface is removed by using an etching reagent after a predefined time interval. The etching reagent consists of NH4F by 37wt% or more, HF by 0.5wt% or less and water by 0.1wt% or less.

ADVANTAGE - Inhibits generation of roughness on side face of contact hole and enables effective etching. Prevents conducting defect of wiring and void generation during contact hole formation. Provides reliable semiconductor device.

(19)日本国特許庁（ＪＰ）　(12)**公開特許公報（Ａ）**　(11)特許出願公開番号

特開平9－148301

(43)公開日　平成９年(1997)６月６日

(51)Int.Cl.[6]		識別記号	庁内整理番号	ＦＩ			技術表示箇所
Ｈ０１Ｌ	21/306			Ｈ０１Ｌ	21/306	Ｑ	
	21/308				21/308	Ｇ	
						Ｅ	
	21/768				21/90	Ｃ	

審査請求　有　　請求項の数５　ＯＬ　（全　４　頁）

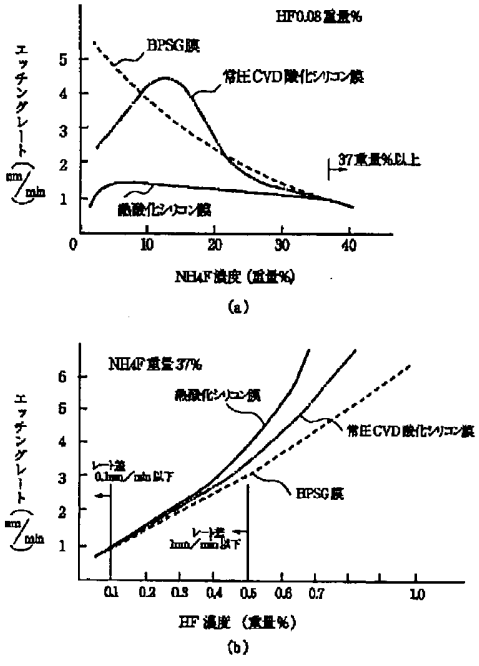
(21)出願番号　特願平7－311229

(22)出願日　平成７年(1995)11月29日

(71)出願人　000004237
日本電気株式会社
東京都港区芝五丁目７番１号
(72)発明者　岡村　正朗
東京都港区芝五丁目７番１号　日本電気株式会社内
(74)代理人　弁理士　京本　直樹　（外２名）

(54)【発明の名称】　半導体装置の製造方法とエッチング液

(57)【要約】
【課題】半導体装置の製造工程において、多層膜に開孔したコンタクト孔の底部の酸化シリコン膜を除去するため、バッファードフッ酸で処理する場合、ホール側面に凹凸が生じないようにする。
【解決手段】本発明のバッファードフッ酸はNH_4 Ｆ３７重量%以上、ＨＦ０．５重量%以下ないし０．１重量%以下の濃度を有している。
【効果】本発明により多層膜に開孔したコンタクト孔の各膜に対するエッチングレートが等しく、かつエッチングレートが小さいため、コンタクトホール側面に凹凸を生じず制御性のよい処理が可能となる。



1

【特許請求の範囲】

【請求項1】　少なくとも2種類の酸化シリコン系絶縁膜を含む多層膜を半導体基板上に形成し、前記多層膜にコンタクト孔を形成して前記半導体基板を露出させる工程と、しかる後前記露出面の自然酸化膜を除去する工程とを有する半導体装置の製造方法において、0重量%超過、0．5重量%以下のHF、少なくとも37重量%のNH_4 F及び残部水からなるエッチング液を用いて前記自然酸化膜を除去することを特徴とする半導体装置の製造方法。

【請求項2】　熱酸化シリコン膜、BPSG膜および常圧CVD酸化シリコン膜のうち少なくとも2種類を含む多層膜である請求項1記載の半導体装置の製造方法。

【請求項3】　エッチング液に界面活性剤が添加されている請求項1又は2記載の半導体装置の製造方法。

【請求項4】　0重量%超過、0．1重量%以下のHF、少なくとも37重量%のNH_4 F及び残部水からなることを特徴とする酸化シリコン系絶縁膜用のエッチング液。

【請求項5】　界面活性剤が添加されている請求項4記載のエッチング液。

【発明の詳細な説明】

【0001】

【発明の属する技術分野】本発明は半導体装置の製造方法とエッチング液に関し、特に半導体基板上の絶縁性の多層膜にコンタクト孔を形成した後の処理方法とその処理に使用するエッチング液に関する。

【0002】

【従来の技術】従来のバッファードフッ酸としては、特公平3－17372号公報に示されたHF0．1～10重量%，NH_4 F15～40重量%、残部が界面活性剤を添加した水というものとまた、特公平3－45533号公報に示された、横軸にHF濃度、縦軸にNH_4 F濃度をとったグラフのA（HF6．1%，NH_4 F32．5%）、B（HF5．1%，HN_4 F12．4%）、C（HF5．9%，NH_4F10%）、D（HF7%，NH_4 F26%）の4点を結んだ四角形の範囲内のHF，NH_4 F、残部水でなるというものがある。

【0003】

【発明が解決しようとする課題】この、従来の濃度のバッファードフッ酸を用いて、コンタクト孔開孔後の底部の自然酸化膜を除去する工程を行うとする。

【0004】たとえば、図3に示すように、熱酸化シリコン膜（シリコンを熱酸化した酸化シリコン膜）3、BPSG（ボロンリンケイ酸ガラス）4－1，4－2、常圧CVD酸化シリコン膜（常圧CVD法で堆積した酸化シリコン膜）5からなる多層膜に0．35μm径のコンタクト孔1を選択性のないドライエッチング法で開孔し、その後処理を行うとすると、特公平3－45533号公報に示されたバッファードフッ酸では、エッチング

2

レートが、20℃で熱酸化シリコン膜に対して80～100nm／minと速すぎ、形成済のコンタクト孔を拡大してしまうためこの用途には適さない。特公平3－17372号公報に示されたバッファードフッ酸のうち、たとえば130BHF（HF1．61%，NH_4 F38．7%）を用いて処理を行うと、絶縁性多層膜の各膜のエッチングレートの違いによって、コンタクト孔側面に凹凸が生じる。

【0005】図2は、このバッファードフッ酸で30秒間処理した時のコンタクト孔を示したものであるが、各酸化シリコン系膜のエッチングレートの差により、側面に10～20nmの凹凸が生じている。このため、この後コンタクト孔にスパッタで金属配線用の金属膜を被着しようとした場合、凹凸部で段切れを起こし導通不良となったり、CVD法によりコンタクト孔を導電膜で埋込んでプラグコンタクトを形成する場合ボイドの発生する原因となったりするという問題点があった。

【0006】従って本発明の目的は、酸化シリコン系絶縁膜を少なくとも2種類含む多層膜に設けられたコンタクト孔底部の自然酸化膜を前記コンタクト孔側面に凹凸が発生するのを抑制しつつ除去できる半導体装置の製造方法とエッチング液を提供することにある。

【0007】

【課題を解決するための手段】本発明の半導体装置の製造方法は、少なくとも2種類の酸化シリコン系絶縁膜を含む多層膜を半導体基板上に形成し、前記多層膜にコンタクト孔を形成して前記半導体基板を露出させる工程と、しかる後前記露出面の自然酸化膜を除去する工程とを有する半導体装置の製造方法において、0重量%超過、0．5重量%以下のHF、少なくとも37重量%のNH_4 F及び残部水からなるエッチング液を用いて前記自然酸化膜を除去するというものである。

【0008】この場合、多層膜を熱酸化シリコン膜、BPSG膜および常圧CVD酸化シリコン膜のうち少なくとも2種類を含んで形成することができる。又、エッチング液に界面活性剤を添加してもよい。

【0009】本発明のエッチング液は、0重量%超過、0．1重量%以下のHF、少なくとも37重量%のNH_4 F及び残部水からなることを特徴とする酸化シリコン系絶縁膜用のエッチング液である。

【0010】この場合、界面活性剤を添加してもよい。

【0011】HF濃度が0．5重量%以下と低く、NH_4 F濃度が37%以上と高いので緩衝作用が強く各種の酸化シリコン系絶縁膜に対するエッチングレートの差を1nm／min以下となる。

【0012】

【発明の実施の形態】図1は各種酸化シリコン系絶縁膜のバッファードフッ酸によるエッチングレートを示すグラフである。すなわち図1（a）はHFの濃度を0．08重量%に保ち、NH_4 F濃度を変化させたときのグラ

フ、図1（b）はNH_4Fの濃度を37重量%に保ち、HF濃度を変化させたときのグラフである。いずれの場合も残部は水である。BPSG膜のリン濃度は4．5モル%、ボロン濃度は10．5%、常圧CVD酸化シリコン膜の成膜温度は400℃である。この実験結果からすると、0重量%超過、0．5重量%以下のHF、少なくとも37%重量%のNH_4F及び残部水からなるエッチング液に対するエッチレート差は1nm／min以下になり、更にHFの濃度を0．1重量%以下にすると0．1nm／min以下になることが判る。NH_4Fの濃度の上限は、溶解度とその温度依存性を考慮すると40重量%がせいぜいである。

【0013】次に、本発明の半導体装置の製造方法の一実施の形態について述べる。

【0014】図2に示すように、Si基板2表面に、熱酸化シリコン膜（例えばMOSトランジスタのドレイン領域の表面を覆っているものとする）、BPSG膜4－1、常圧CVD酸化シリコン膜（常圧CVD法により形成した酸化シリコン膜）5、BPSG膜4－2を順次に形成し、これらの酸化シリコン系絶縁膜に対して選択性のないドライエッチング法により、0．35μm径（設計ルール0．35μm）のコンタクト孔1Aを形成し、Si基板1を露出させる。このときSi基板1の表面は多少削られる。次に、ドライエッチング装置から取り出し、次の配線層形成までの間、空気中に放置される。配線層形成の直前に、Si基板面の自然酸化膜を除去するのにHF濃度が0．5重量%、NH_4F濃度が37重量%、残部水でなるバッファードフッ酸を使用する。自然酸化膜の厚さは放置される時間等によって異なっているが約1～2nmであり、3分～5分程度で除去できる。従って、コンタクト孔1Aの側面の凹凸は5nm以下に抑制される。これはコンタクト孔径に比較して十分に小さいので配線層を形成する場合の段切れや導通不良もしくは埋込みプラグ形成時のボイドの発生は若しく減少する。

【0015】なお、300～500℃で成膜した常圧CVD酸化シリコン膜、リン濃度2モル%～7モル%、ボロン濃度6モル%～15%のBPSG膜を含む多層膜にコンタクト孔を設ける場合についても、本実施の形態に準じる結果が得られた。更に、本実施の形態に含まれな

いPSG膜や高温酸化シリコン膜（HTO膜）などその他の酸化シリコン系絶縁膜を含む多層膜であっても、従来例に比べてコンタクト孔側面の凹凸を少なくできることは明白である。又、バッファードフッ酸に界面活性剤を添加することは普通に行なわれているが、本発明の場合にもそうしてもよい。その場合の界面活性剤としては、公知のもの、例えば特公平3－17372号公報に記載されているものを使用できる。すなわち、脂肪族カルボン酸$C_nH_{2n+1}COOH$（nは5～11の整数）、脂肪族カルボン酸の塩$C_nH_{2n+1}COONH_3R$（nは5～11の整数、Rは水素原子または炭素数5～10のアルキル基）、脂肪族アミン$C_mH_{2m+1}NH_2$（mは7～14の整数）又は脂肪族アルコール$C_nH_{2n+1}OH$（nは6～12の整数）もしくはこれらの混合物である界面活性剤を使用できる。添加量は10～10000ppmが適当である。

【0016】

【発明の効果】以上説明したように、本発明のバッファードフッ酸は、各種の酸化シリコン系絶縁膜についてはほぼ等しいエッチングレートを持ち、かつエッチングレートが充分小さいため、コンタクト孔側面にできる凹凸を抑制しつつ制御性のよいエッチングが可能である。これによって、コンタクト部での配線の導通不良や、コンタクト孔埋込み時のボイド等を防ぐことができ、半導体装置の信頼性向上につながるという効果を有する。

【図面の簡単な説明】

【図1】本発明について説明するためのバッファードフッ酸のエッチングレートのNH_4F濃度依存性を示すグラフ（図1（a））及びHF濃度依存性を示すグラフ（図1（b））である。

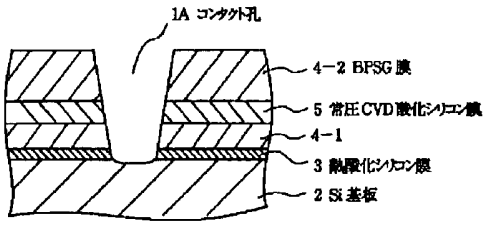
【図2】本発明の半導体装置の製造方法について説明するための断面図である。

【図3】従来例の問題点の説明に使用する断面図である。

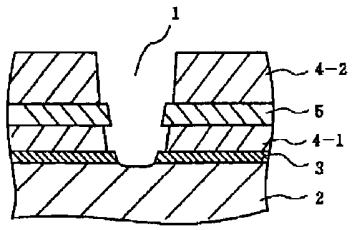
【符号の説明】

1，1A　コンタクト孔
2　Si基板
3　熱酸化シリコン膜
4－1，4－2　BPSG膜
5　常圧CVD酸化シリコン膜

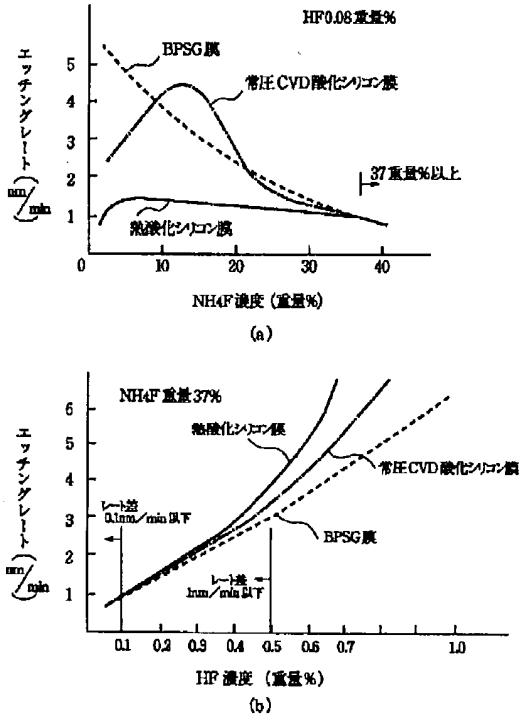
【図2】



【図3】



【図1】


HF0.08重量%
BPSG膜
常圧CVD酸化シリコン膜
37重量%以上
熱酸化シリコン膜
エッチングレート nm/min
NH4F濃度（重量%）
(a)
NH4F重量37%
熱酸化シリコン膜
常圧CVD酸化シリコン膜
BPSG膜
レート差 0.1nm/min以下
レート差 1nm/min以下
HF濃度（重量%）
(b)

* NOTICES *

JP09-148301

1.This document has been translated by computer. So the translation may not reflect the original precisely.
2.**** shows the word which can not be translated.
3.In the drawings, any words are not translated.

CLAIMS

[Claim(s)]
[Claim 1] The process at which the multilayer containing at least two kinds of silicon oxide system insulator layers is formed on a semi-conductor substrate, a contact hole is formed in said multilayer, and said semi-conductor substrate is exposed, In the manufacture approach of a semiconductor device of having the process which removes the natural oxidation film of the appropriate account exposed surface of back to front The manufacture approach of the semiconductor device characterized by removing said natural oxidation film using the etching reagent which consists of an excess of 0 % of the weight, 0.5 or less % of the weight of HF, NH[at least 37% of the weight of]4 F, and remainder water.
[Claim 2] The manufacture approach of the semiconductor device according to claim 1 which is a multilayer including at least two kinds in the thermal oxidation silicon film, the BPSG film, and the ordinary pressure CVD silicon oxide film.
[Claim 3] The manufacture approach of a semiconductor device according to claim 1 or 2 that the surfactant is added by the etching reagent.
[Claim 4] The etching reagent for silicon oxide system insulator layers characterized by consisting of an excess of 0 % of the weight, 0.1 or less % of the weight of HF, NH[at least 37% of the weight of]4 F, and remainder water.
[Claim 5] The etching reagent according to claim 4 with which the surface active agent is added.

[Translation done.]

* NOTICES *

1.This document has been translated by computer. So the translation may not reflect the original precisely.
2.**** shows the word which can not be translated.
3.In the drawings, any words are not translated.

DETAILED DESCRIPTION

[Detailed Description of the Invention]
[0001]
[Field of the Invention] This invention relates to the etching reagent used for an art and processing after forming a contact hole in the insulating multilayer especially on a semi-conductor substrate about the manufacture approach of a semiconductor device, and an etching reagent.
[0002]
[Description of the Prior Art] 0.1 - 10 % of the weight of HF, four F15 - 40 % of the weight of NH(s) shown in JP,3-17372,B as conventional buffered fluoric acid, The remainder was indicated to be a thing called the water which added the surfactant to JP,3-45533,B again. A of the graph which took HF concentration along the axis of abscissa, and took NH4 F concentration along the axis of ordinate (HF6.1%, four F32.5% of NH(s)), There is a thing of becoming with HF of the square to which four points of B (HF5.1%, four F12.4% of HN(s)), C (HF5.9%, NH4F10%), and D (HF7%, four F26% of NH(s)) were connected within the limits, NH4 F, and remainder water.
[0003]
[Problem(s) to be Solved by the Invention] Suppose that the process which removes the natural oxidation film of the pars basilaris ossis occipitalis after contact hole puncturing is performed using the buffered fluoric acid of this conventional concentration.
[0004] For example, as shown in drawing 3 Thermal oxidation silicon film (silicon) The contact hole 1 of the diameter of 0.35 micrometer is punctured by the dry etching method without selectivity to the multilayer which consists of the silicon oxide film 3 oxidized thermally, BPSG (boron phosphorus silicic-acid glass) 4-1, 4-2, and ordinary pressure CVD silicon oxide film (silicon oxide film deposited with the ordinary pressure CVD method) 5. Supposing it performs that after treatment, in order that an etching rate may expand a contact hole [finishing / formation / it is too as quick as 80 - 100 nm/min to the thermal oxidation silicon film at 20 degrees C and], by the buffered fluoric acid shown in JP,3-45533,B, it is not suitable for this application. If it processes among the buffered fluoric acid shown in JP,3-17372,B using 130BHF (HF1.61%, four F38.7% of NH(s)), irregularity will arise on a contact hole side face by the difference in the etching rate of each film of an insulating multilayer.
[0005] Although drawing 2 shows the contact hole when processing for 30 seconds by this buffered fluoric acid, the irregularity of 10-20nm has produced it on the side face according to the difference of the etching rate of each silicon oxide system film. For this reason, there was a trouble of becoming lifting defective continuity about a stage piece in the concavo-convex section when it is going to put the metal membrane for metal wiring on a contact hole by the spatter after this, or becoming the cause which a void generates when embedding a contact hole by the electric conduction film with a CVD method and forming plug contact.
[0006] Therefore, the object of this invention is to offer the manufacture approach of a semiconductor device removable [controlling that irregularity generates the natural oxidation film of the contact hole pars basilaris ossis occipitalis prepared in the multilayer containing at least two kinds of silicon oxide system insulator layers on said contact hole side face], and an etching reagent.

[0007]
[Means for Solving the Problem] The process at which the manufacture approach of the semiconductor device of this invention forms the multilayer containing at least two kinds of silicon oxide system insulator layers on a semi-conductor substrate, a contact hole is formed in said multilayer, and said semi-conductor substrate is exposed, In the manufacture approach of a semiconductor device of having the process which removes the natural oxidation film of the appropriate account exposed surface of back to front, said natural oxidation film is removed using the etching reagent which consists of an excess of 0 % of the weight, 0.5 or less % of the weight of HF, NH[at least 37% of the weight of]4 F, and remainder water.
[0008] In this case, a multilayer can be formed including at least two kinds in the thermal oxidation silicon film, the BPSG film, and the ordinary pressure CVD silicon oxide film. Moreover, a surfactant may be added to an etching reagent.
[0009] The etching reagent of this invention is an etching reagent for silicon oxide system insulator layers characterized by consisting of an excess of 0 % of the weight, 0.1 or less % of the weight of HF, NH[at least 37% of the weight of]4 F, and remainder water.
[0010] In this case, a surfactant may be added.
[0011] HF concentration is as low as 0.5 or less % of the weight, and since NH4 F concentration is high, it becomes 37% or more with 1 or less nm/min about the difference of the etching rate to various kinds of silicon oxide system insulator layers with strong buffer action.
[0012]
[Embodiment of the Invention] Drawing 1 is a graph which shows the etching rate by the buffered fluoric acid of various silicon oxide system insulator layers. That is, drawing 1 (a) is a graph when maintaining the concentration of HF to 0.08% of the weight, and the graph when changing NH4 F concentration and drawing 1 (b) maintaining the concentration of NH4 F to 37% of the weight, and changing HF concentration. In any case, the remainder is water. The Lynn concentration of the BPSG film is [the membrane formation temperature of the ordinary pressure CVD silicon oxide film of 4.5-mol % and boron concentration] 400 degrees C 10.5%. Considering this experimental result, they are an excess of 0 % of the weight, 0.5 or less % of the weight of HF, and at least 37%% of the weight of NH4. And when the dirty rate difference over the etching reagent which consists of remainder water becomes 1 or less nm/min and concentration of HF is further carried out to 0.1 or less % of the weight, it turns out that it becomes 0.1 or less nm/min. if solubility and its temperature dependence are taken into consideration, 40 % of the weight will come out of the upper limit of the concentration of NH4 F at most.
[0013] Next, the gestalt of 1 implementation of the manufacture approach of the semiconductor device of this invention is described.
[0014] As shown in drawing 2 , on Si substrate 2 front face The thermal oxidation silicon film (for example, the front face of the drain field of an MOS transistor shall be covered), By the dry etching method which forms the BPSG film 4-1, the ordinary pressure CVD silicon oxide film (silicon oxide film formed with the ordinary pressure CVD method) 5, and the BPSG film 4-2 one by one, and does not have selectivity to these silicon oxide system insulator layers Contact hole 1A of the diameter (design rule 0.35micrometer) of 0.35 micrometer is formed, and the Si substrate 1 is exposed. At this time, some front faces of the Si substrate 1 are deleted. Next, it is left from a dry etching system before ejection and the next wiring layer formation and in air. NH4 F concentration uses [HF concentration] the buffered fluoric acid which becomes with remainder water 37% of the weight 0.5% of the weight for removing the natural oxidation film of Si substrate side just before wiring layer formation. Although the thickness of the natural oxidation film changes with time amount left, it is about 1-2nm, and it can be removed in 3 minutes - about 5 minutes. Therefore, the irregularity of the side face of contact hole 1A is controlled by 5nm or less. Since this is fully small as compared with a contact aperture, generating of the stage piece in the case of forming a wiring layer, defective continuity, or the void at the time of pad plug formation is ******(ed).
[0015] In addition, the result which applies to the gestalt of this operation correspondingly also about the

case where a contact hole is prepared in the multilayer containing the BPSG film (ordinary pressure CVD silicon oxide film [which formed membranes at 300-500 degrees C], and Lynn concentration % of two mols -, and seven-mol %, and boron concentration 6 mol %-15%) was obtained. Furthermore, even if it is a multilayer containing other silicon oxide system insulator layers, such as PSG film, high-temperature-oxidation silicon film (HTO film), etc. which are not contained in the gestalt of this operation, it is clear that irregularity of a contact hole side face can be lessened compared with the conventional example. Moreover, although adding a surfactant to buffered fluoric acid is performed ordinarily, also in the case of this invention, you may do so. As a surfactant in that case, a well-known thing, for example, the thing indicated by JP,3-17372,B, can be used. Namely, aliphatic-carboxylic-acid Cn H2n+1C00H (n is the integer of 5-11), salt Cn H2n+1C00NH3 R (n -- the integer of 5-11 --) of aliphatic carboxylic acid R can use the surfactant which are a hydrogen atom or the alkyl group of carbon numbers 5-10, fatty amine Cm H2m+1NH2, fatty alcohol Cn H2n+1OH(s) (n is the integer of 6-12), or such mixture. 10-10000 ppm is suitable for an addition.

[0016]

[Effect of the Invention] As explained above, good etching of a controllability is possible for it, the buffered fluoric acid of this invention controlling the irregularity which has an etching rate almost equal about various kinds of silicon oxide system insulator layers, and is made on a contact hole side face since the etching rate is sufficiently small. By this, the defective continuity of wiring in the contact section, the void at the time of a contact hole pad, etc. can be prevented, and it has the effectiveness of leading to the improvement in dependability of a semiconductor device.

[Translation done.]

* NOTICES *

1.This document has been translated by computer. So the translation may not reflect the original precisely.
2.**** shows the word which can not be translated.
3.In the drawings, any words are not translated.

TECHNICAL FIELD

[Field of the Invention] This invention relates to the etching reagent used for an art and processing after forming a contact hole in the insulating multilayer especially on a semi-conductor substrate about the manufacture approach of a semiconductor device, and an etching reagent.

[Translation done.]

* NOTICES *

PRIOR ART

[Description of the Prior Art] It is A (HF6.1%, four F32.5% of NH(s)) of the graph which took HF concentration along the axis of abscissa, and took NH4 F concentration along the axis of ordinate by which it was indicated in JP,3-45533,B as a thing called the water with which 0.1 - 10 % of the weight of HF shown in JP,3-17372,B, four F15 - 40 % of the weight of NH(s), and the remainder added the surfactant as conventional buffered fluoric acid again, There is a thing of becoming with HF of the square to which four points of B (HF5.1%, four F12.4% of HN(s)), C (HF5.9%, NH4F10%), and D (HF7%, four F26% of NH(s)) were connected within the limits, NH4 F, and remainder water.

[Translation done.]

* NOTICES *

1.This document has been translated by computer. So the translation may not reflect the original precisely.
2.**** shows the word which can not be translated.
3.In the drawings, any words are not translated.

EFFECT OF THE INVENTION

[Effect of the Invention] As explained above, good etching of a controllability is possible for it, the buffered fluoric acid of this invention controlling the irregularity which has an etching rate almost equal about various kinds of silicon oxide system insulator layers, and is made on a contact hole side face since the etching rate is sufficiently small. By this, the defective continuity of wiring in the contact section, the void at the time of a contact hole pad, etc. can be prevented, and it has the effectiveness of leading to the improvement in dependability of a semiconductor device.

[Translation done.]

* NOTICES *

TECHNICAL PROBLEM

[Problem(s) to be Solved by the Invention] Suppose that the process which removes the natural oxidation film of the pars basilaris ossis occipitalis after contact hole puncturing is performed using the buffered fluoric acid of this conventional concentration.
[0004] For example, as shown in drawing 3 Thermal oxidation silicon film (silicon) The contact hole 1 of the diameter of 0.35 micrometer is punctured by the dry etching method without selectivity to the multilayer which consists of the silicon oxide film 3 oxidized thermally, BPSG (boron phosphorus silicic-acid glass) 4-1, 4-2, and ordinary pressure CVD silicon oxide film (silicon oxide film deposited with the ordinary pressure CVD method) 5. Supposing it performs that after treatment, in order that an etching rate may expand a contact hole [finishing / formation / it is too as quick as 80 - 100 nm/min to the thermal oxidation silicon film at 20 degrees C and], by the buffered fluoric acid shown in JP,3-45533,B, it is not suitable for this application. If it processes among the buffered fluoric acid shown in JP,3-17372,B using 130BHF (HF1.61%, four F38.7% of NH(s)), irregularity will arise on a contact hole side face by the difference in the etching rate of each film of an insulating multilayer.
[0005] Although drawing 2 shows the contact hole when processing for 30 seconds by this buffered fluoric acid, the irregularity of 10-20nm has produced it on the side face according to the difference of the etching rate of each silicon oxide system film. For this reason, there was a trouble of becoming lifting defective continuity about a stage piece in the concavo-convex section when it is going to put the metal membrane for metal wiring on a contact hole by the spatter after this, or becoming the cause which a void generates when embedding a contact hole by the electric conduction film with a CVD method and forming plug contact.
[0006] Therefore, the object of this invention is to offer the manufacture approach of a semiconductor device removable [controlling that irregularity generates the natural oxidation film of the contact hole pars basilaris ossis occipitalis prepared in the multilayer containing at least two kinds of silicon oxide system insulator layers on said contact hole side face], and an etching reagent.

[Translation done.]

* NOTICES *

MEANS

[Means for Solving the Problem] The process at which the manufacture approach of the semiconductor device of this invention forms the multilayer containing at least two kinds of silicon oxide system insulator layers on a semi-conductor substrate, a contact hole is formed in said multilayer, and said semi-conductor substrate is exposed, In the manufacture approach of a semiconductor device of having the process which removes the natural oxidation film of the appropriate account exposed surface of back to front, said natural oxidation film is removed using the etching reagent which consists of an excess of 0 % of the weight, 0.5 or less % of the weight of HF, NH[at least 37% of the weight of]4 F, and remainder water.
[0008] In this case, a multilayer can be formed including at least two kinds in the thermal oxidation silicon film, the BPSG film, and the ordinary pressure CVD silicon oxide film. Moreover, a surfactant may be added to an etching reagent.
[0009] The etching reagent of this invention is an etching reagent for silicon oxide system insulator layers characterized by consisting of an excess of 0 % of the weight, 0.1 or less % of the weight of HF, NH[at least 37% of the weight of]4 F, and remainder water.
[0010] In this case, a surfactant may be added.
[0011] HF concentration is as low as 0.5 or less % of the weight, and since NH4 F concentration is high, it becomes 37% or more with 1 or less nm/min about the difference of the etching rate to various kinds of silicon oxide system insulator layers with strong buffer action.
[0012]
[Embodiment of the Invention] Drawing 1 is a graph which shows the etching rate by the buffered fluoric acid of various silicon oxide system insulator layers. That is, drawing 1 (a) is a graph when maintaining the concentration of HF to 0.08% of the weight, and the graph when changing NH4 F concentration and drawing 1 (b) maintaining the concentration of NH4 F to 37% of the weight, and changing HF concentration. In any case, the remainder is water. The Lynn concentration of the BPSG film is [the membrane formation temperature of the ordinary pressure CVD silicon oxide film of 4.5-mol % and boron concentration] 400 degrees C 10.5%. Considering this experimental result, they are an excess of 0 % of the weight, 0.5 or less % of the weight of HF, and at least 37%% of the weight of NH4. And when the dirty rate difference over the etching reagent which consists of remainder water becomes 1 or less nm/min and concentration of HF is further carried out to 0.1 or less % of the weight, it turns out that it becomes 0.1 or less nm/min. if solubility and its temperature dependence are taken into consideration, 40 % of the weight will come out of the upper limit of the concentration of NH4 F at most.
[0013] Next, the gestalt of 1 implementation of the manufacture approach of the semiconductor device of this invention is described.
[0014] As shown in drawing 2 , on Si substrate 2 front face The thermal oxidation silicon film (for example, the front face of the drain field of an MOS transistor shall be covered), By the dry etching method which forms the BPSG film 4-1, the ordinary pressure CVD silicon oxide film (silicon oxide film formed with the ordinary pressure CVD method) 5, and the BPSG film 4-2 one by one, and does

not have selectivity to these silicon oxide system insulator layers Contact hole 1A of the diameter (design rule 0.35micrometer) of 0.35 micrometer is formed, and the Si substrate 1 is exposed. At this time, some front faces of the Si substrate 1 are deleted. Next, it is left from a dry etching system before ejection and the next wiring layer formation and in air. NH4 F concentration uses [HF concentration] the buffered fluoric acid which becomes with remainder water 37% of the weight 0.5% of the weight for removing the natural oxidation film of Si substrate side just before wiring layer formation. Although the thickness of the natural oxidation film changes with time amount left, it is about 1-2nm, and it can be removed in 3 minutes - about 5 minutes. Therefore, the irregularity of the side face of contact hole 1A is controlled by 5nm or less. Since this is fully small as compared with a contact aperture, generating of the stage piece in the case of forming a wiring layer, defective continuity, or the void at the time of pad plug formation is ******(ed).

[0015] In addition, the result which applies to the gestalt of this operation correspondingly also about the case where a contact hole is prepared in the multilayer containing the BPSG film (ordinary pressure CVD silicon oxide film [which formed membranes at 300-500 degrees C], and Lynn concentration % of two mols -, and seven-mol %, and boron concentration 6 mol %-15%) was obtained. Furthermore, even if it is a multilayer containing other silicon oxide system insulator layers, such as PSG film, high-temperature-oxidation silicon film (HTO film), etc. which are not contained in the gestalt of this operation, it is clear that irregularity of a contact hole side face can be lessened compared with the conventional example. Moreover, although adding a surfactant to buffered fluoric acid is performed ordinarily, also in the case of this invention, you may do so. As a surfactant in that case, a well-known thing, for example, the thing indicated by JP,3-17372,B, can be used. Namely, aliphatic-carboxylic-acid Cn H2n+1C00H (n is the integer of 5-11), salt Cn H2n+1C00NH3 R (n -- the integer of 5-11 --) of aliphatic carboxylic acid R can use the surfactant which are a hydrogen atom or the alkyl group of carbon numbers 5-10, fatty amine Cm H2m+1NH2, fatty alcohol Cn H2n+1OH(s) (n is the integer of 6-12), or such mixture. 10-10000 ppm is suitable for an addition.

[Translation done.]

* NOTICES *

1.This document has been translated by computer. So the translation may not reflect the original precisely.
2.**** shows the word which can not be translated.
3.In the drawings, any words are not translated.

DESCRIPTION OF DRAWINGS

[Brief Description of the Drawings]
[Drawing 1] It is the graph (drawing 1 (b)) which shows the graph (drawing 1 (a)) and HF concentration dependency which show the NH4 F concentration dependency of the etching rate of the buffered fluoric acid for explaining this invention.
[Drawing 2] It is a sectional view for explaining the manufacture approach of the semiconductor device of this invention.
[Drawing 3] It is the sectional view used for explanation of the trouble of the conventional example.
[Description of Notations]
1 1A Contact hole
2 Si Substrate
3 Thermal Oxidation Silicon Film
4-1, 4-2 BPSG film
5 Ordinary Pressure CVD Silicon Oxide Film

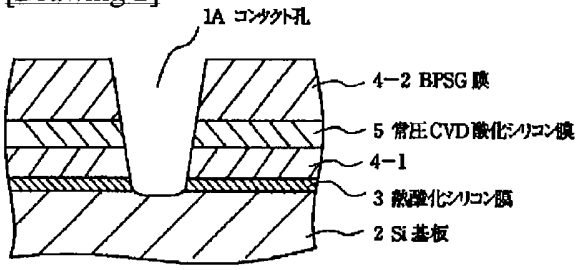
[Translation done.]

* NOTICES *

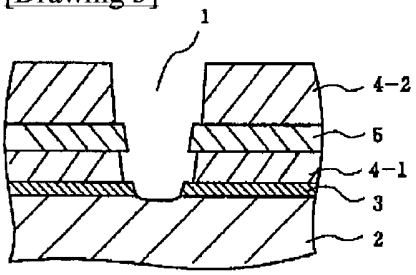
1.This document has been translated by computer. So the translation may not reflect the original precisely.
2.**** shows the word which can not be translated.
3.In the drawings, any words are not translated.

DRAWINGS

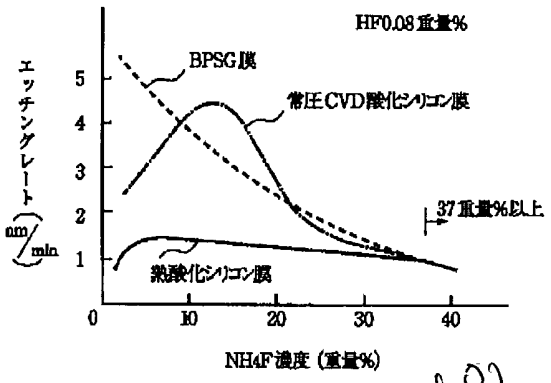
[Drawing 2]



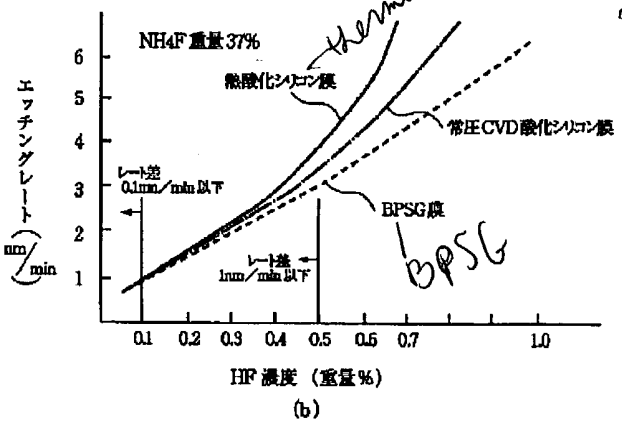
[Drawing 3]



[Drawing 1]



(a)



(b)

thermal SiO_2

BPSG

For (0.1–0.5) wt% HF / 37 wt.% NH_4F
BPSG + thermal SiO_2 have
the same etch rate (1–3) $\frac{nm}{min}$
$\frac{(10\text{–}30)\ \text{Å}}{min}$

[Translation done.]